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REMARKS

Applicants have studied the Office Action dated November 20, 2002 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 15-25 are pending.¹ Claims 15 and 16 have been amended, and new claims 20-25 have been added. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

Claim 15 was rejected under 35 U.S.C. § 102(b) as being anticipated by Greco et al. (U.S. Patent No. 5,371,017). Claim 15 was also rejected under 35 U.S.C. § 102(c) as being anticipated by Koyama (U.S. Patent No. 5,981,377). These rejections are respectfully traversed.

The present invention is directed to providing an integrated circuit having substantially constant electrical resistance between superposed vias. One embodiment of the present invention provides an integrated circuit of the type that has metallization levels separated by dielectric layers and metallized vias connecting lines of different metallization levels. The integrated circuit includes at least first and second metallization levels, at least first and second superposed dielectric layers located above the first metallization level, and a third dielectric layer located above the first and second dielectric layers. The first dielectric layer is located on the first metallization level, and at least one electrical connection element is provided in the third dielectric layer and passes through the second dielectric layer until it comes into contact with the first dielectric layer. Because the first dielectric layer is located on the first metallization level and the electrical connection element passes through the second dielectric layer until it comes into contact with the first dielectric layer, the thickness of lines and electrical resistance are satisfactorily controlled.

¹ Applicants again note that claims 1-14 were canceled in paragraph 5 of the "Request for Filing a Divisional Application" filed with the present application. Thus, only claims 15-19 were pending before the filing of this Amendment.

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The Greco reference discloses an integrated circuit having an inorganic dielectric between interconnection layers. The Koyama reference discloses a semiconductor device having an improved trench interconnection structure. However, neither Greco nor Koyama discloses an integrated circuit that includes at least first and second superposed dielectric layers located above a first metallization level with the first dielectric layer being located on the first metallization level, a third dielectric layer located above the first and second dielectric layers, and at least one electrical connection element provided in the third dielectric layer and passing through the second dielectric layer until it comes into contact with the first dielectric layer, as is recited in amended claim 15.

Greco discloses an integrated circuit having four dielectric layers located between two metallization levels. More specifically, the integrated circuit has a first metallization level 310, a first dielectric layer 116, a second dielectric layer 126, a third dielectric layer 210, a fourth dielectric layer 220, and then a second metallization level 330, as shown in Figure 4. A first via 325 extends from the first metallization level 310 through the first and second dielectric layers 116 and 126. A second via 212 extends from the second metallization level 330 through the fourth and third dielectric layers 220 and 210. Thus, the via provided in the dielectric layers above the second dielectric layer does not pass through the second dielectric layer. In other words, the integrated circuit of Greco does not include first and second superposed dielectric layers with the first dielectric layer located on a first metallization level, and an electrical connection element provided in a higher dielectric layer and passing through the second dielectric layer.

Koyama discloses an integrated circuit having five dielectric layers located between two metallization levels. More specifically, the integrated circuit has a first metallization level formed in dielectric layer 50 that includes line 51, as shown in Figure 5F. Above the first metallization level the integrated circuit has a first dielectric film 51a, a second dielectric layer 52a, a third dielectric layer 52b, and then a second metallization level formed in two dielectric layers 52c and 52d. A via 55 extends from the first metallization level to the second metallization level and passes through the lower dielectric layer 50, the first dielectric film 51a, the second and third dielectric layers 52a and 52b, and one of the upper dielectric layers 52c. A

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filled trench 58 extends through the two upper dielectric layers 52c and 52d. Thus, there is not an electrical connection element provided in the dielectric layers above the second dielectric layer and passing through the second dielectric layer. In other words, the integrated circuit of Koyama does not include first and second superposed dielectric layers with the first dielectric layer located on a first metallization level, and an electrical connection element provided in a higher dielectric layer and passing through the second dielectric layer.

In contrast, in the embodiment of the present invention recited in amended claim 15, the integrated circuit includes first and second superposed dielectric layers located above a first metallization level, with the first dielectric layer being located on the first metallization level. The integrated circuit also includes a third dielectric layer located above the first and second dielectric layers, and at least one electrical connection element provided in the third dielectric layer and passing through the second dielectric layer until it comes into contact with the first dielectric layer. Thus, the integrated circuit includes first and second superposed dielectric layers with the first dielectric layer located on a first metallization level, and an electrical connection element in a dielectric layer above the second dielectric layer and passing through the second dielectric layer.

Neither Greco nor Koyama teaches or suggests an integrated circuit having first and second superposed dielectric layers with the first dielectric layer located on a first metallization level, and an electrical connection element provided in a higher dielectric layer and passing through the second dielectric layer. Applicants believe that the differences between Greco, Koyama, and the present invention are clear in amended claim 15, which sets forth an integrated circuit according to one embodiment of the present invention. Therefore, claim 15 distinguishes over the Greco and Koyama references, and the rejections of this claim under 35 U.S.C. § 102(b) and 35 U.S.C. § 102(e) should be withdrawn.

Claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Greco et al. or Koyama. This rejection is respectfully traversed.

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As explained above, neither Greco nor Koyama teaches or suggests the integrated circuit recited in amended claim 15. Therefore, amended claim 15 distinguishes over the Greco and Koyama references, and thus, claim 18 (which depends from claim 15) also distinguishes over the Greco and Koyama references. Therefore, it is respectfully submitted that the rejection of claim 18 under 35 U.S.C. § 103(a) should be withdrawn.

Applicants thank the Examiner for indicating that claims 16, 17, and 19 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims. Claim 16 has been rewritten in independent form, and claim 17 depends from claim 16. Additionally, claim 19 depends from amended claim 15, which Applicants respectfully submit is allowable over the art of record. Accordingly, it is respectfully submitted that claims 16, 17, and 19 are in condition for allowance.

Claims 20-25 have been added by this amendment, and are provided to further define the invention disclosed in the specification. Claims 20-25 are allowable for at least the reasons set forth above with respect to claims 15-19.

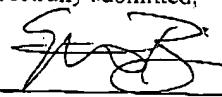
In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

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Respectfully submitted,

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APPENDIX

IN THE CLAIMS:

15. (Amended) An integrated circuit of the type having metallization levels separated by dielectric layers and metallized vias connecting lines of different metallization levels, said integrated circuit comprising:

at least first and second metallization levels;

at least first and second superposed dielectric layers located above the first metallization level, the first dielectric layer being located on the first metallization level;

a third dielectric layer located above the first and second dielectric layers; and

at least one electrical connection element provided in the third dielectric layer and passing through the second dielectric layer until it comes into contact with the first dielectric layer.

16. (Amended) [The] An integrated circuit [as defined in claim 15, further] of the type having metallization levels separated by dielectric layers and metallized vias connecting lines of different metallization levels, said integrated circuit comprising:

at least first and second metallization levels;

at least first and second superposed dielectric layers located above the first metallization level;

a third dielectric layer located above the first and second dielectric layers;

at least one electrical connection element provided in the third dielectric layer and passing through the second dielectric layer until it comes into contact with the first dielectric layer; and

at least one metallized via having an upper surface that is flush with an upper surface of the second dielectric layer.